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Reliability Design of Source/Drain Adaptive Layers in an HV Power nLDMOS

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Abstract

Reliability issues are very important especially for the high-voltage (HV) devices. Unfortunately, an HV nLDMOS is often damaged by a latch-up (LU) problem when it triggered by a transient noise and a bias condition VDD_{max} is greater than that of the device holding-voltage (V_h). The snapback phenomena of the new adding adaptive layers in the source/drain ends of an nLDMOS are investigated in this paper. It is a novel method to reduce the surface field, control the trigger voltage and holding voltage. Experimentally, the right-shifting characteristic of snapback I-V curves depends on new adding P_{ad}, L_{Pad}, N_{ad}, and L_{Nad} parameters, respectively. Eventually, these source/drain adaptive layers of an nLDMOS can effectively improve the LU immunity under an HV operation.

Keywords

Electrostatic Discharge (ESD); Holding Voltage (V_h); Latch-up (LU); nLDMOS; Snapback; Trigger Voltage (V_{t1})

Introduction

HV integrated circuits have been implemented in many applications, such as automotive, air craft, LCD drivers, and industrial robotics. The electrostatic discharge (ESD) and LU reliabilities are two important issues in many kinds of applications. And, it is always found that an n-channel lateral-diffused MOSFET (nLDMOS) shown in Fig. 1 always has a very low holding voltage (V_h), which could suffer the transient-induced LU failure during normal circuit operating condition and inherently weak with respect to ESD stress, especially when such HV nMOSFETs are used in on-chip I/O circuits or power to ground protection cells of an integrated circuit.

This paper discusses the study of an nLDMOS using a systematic approach. DUTs are designed according to a 0.6 μm 80 V/5 V (V_{DS}/V_{GS}) BCD process, the channel length (L) is kept to be 3 μm; channel width (W) is kept a constancy, 50 μm. Variations of specific profiles, in Figs 2 and 3, that lead to higher V_h in the nLDMOS are described. The source/drain-side engineering are attracted much attention to research HV devices recently. Many efforts prevent the Kirk effect and avoids reliability problems. Techniques in our work with a higher dosage can improve the reliability of LDMOS transistors. In addtion, the source/drain-side engineering can suppress substrate noise and prevent LU effect. It's a great method to ensure the HV nLDMOS reliability in many kinds of applications. Therefore, in this paper, our experimental data will demonstrate a novel weak snapback characteristic in the HV nLDMOS device.

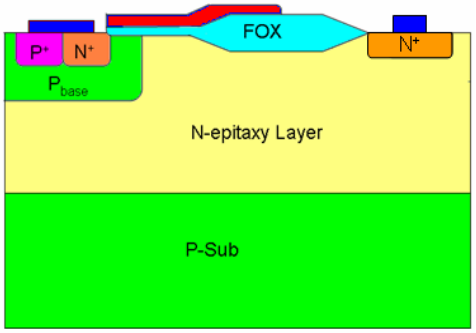

FIG. 1. CONVENTIONAL STRUCTURE OF AN NLDMOS

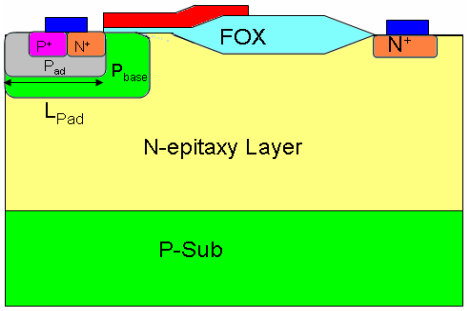

FIG. 2. SOURCE-SIDE P_{ad} LAYER IN AN NLDMOS STRUCTURE

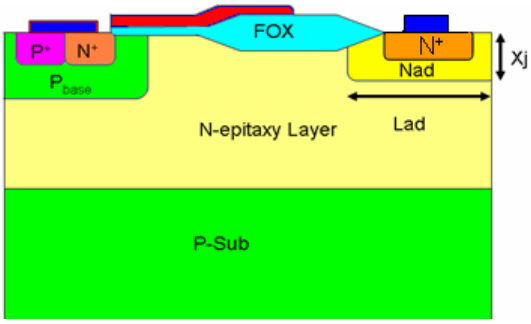

FIG. 3. DRAIN-SIDE N_{ad} LAYER IN AN NLDMOS STRUCTURE

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Device Engineering and I-V Characteristics

Source-side Engineering of an nLDMOS

1) Effect of the P_{ad} Implant Dose

As a current flows through N^+/P_{base} junction when this nLDMOS is triggered by an ESD event that will easily lead to LU happening as shown in Fig. 4. A parasitic BJT turned on by an ESD event is applied on the drain side region and its snapback I-V curve describes this phenomenon. A gate bias induced inversion layer appears on channel surface to turn on MOS to discharge ESD current that will be more faster than the internal equivalent BJT structure (gate-grounded type) triggered on. Extended current flow lines pass through the N_{epi}/P_{sub} space to source region that causes Kirk effect. A P_{ad} layer structure can reduce electrons life time when an ESD event appears and a damaged degradation is excluded in the source region. The electron life time degradation will be a great benefit against Kirk effect. Such that a P_{ad} layer can be added to against ground noise and prevent the LU effect. Increasing the P_{ad} implant dose of source side can raise the recombination rate and the occurrence of punch-trough current is more difficult. A holding voltage was raised to improve LU problem significantly by a P_{ad} implant dose increasing as shown in Fig. 5. But the channel resistance (R_{ch}) was increased by raising the P_{ad} implant dosage; meanwhile, the threshold voltage was increased too.

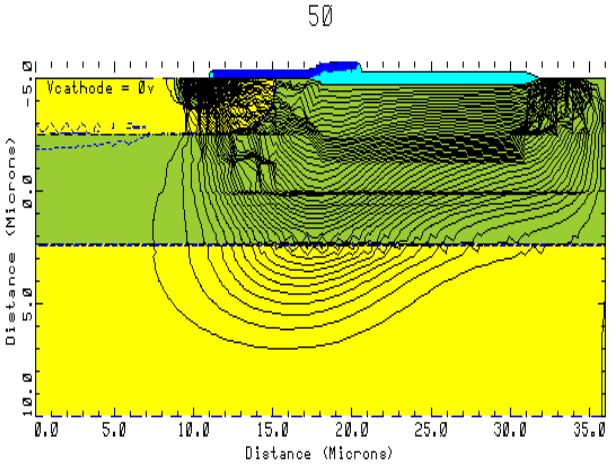

FIG. 4. CURRENT FLOW LINES OF A GATE-GROUNDED NLDMOS AS AN ESD EVENT OCCURRED IN THE DRAIN SIDE

The trigger-on factor β of a parasitic BJT structure is determined by the concentration and length of base region. Adding a base region concentration implies the recombination rate increased. Further, a higher implant doping of P_{ad} layer will affect the channel profile as a P_{ad} position nearby the channel region. In Figs 5 and 6, a higher P_{ad} implant improves LU immunity, however, the R_{on} resistance and threshold voltage raised as well. Eventually, an optimized condition will be traded-off among the holding voltage, R_{on} resistance, and threshold voltage. Furthermore, according to a 0.6 μm 80 V/5 V (V_{DS}/V_g) BCD process, if an implant dosage of source-side P_{ad} is greater than 4.5×10^{15} atoms/cm^2, then its threshold voltage of an nLDMOS will be greater over 5 V on the normal condition. So, in this work, the best dose condition of P_{ad} layer is 4.5×10^{15} atoms/cm^2 as shown in Figs 5 and 6.

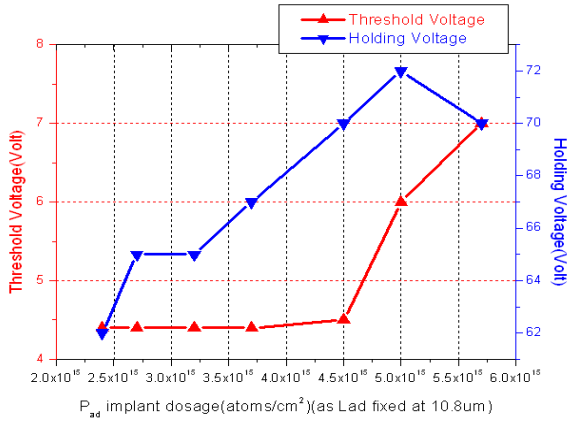

FIG. 5. CHARACTERISTICS OF P_{ad} IMPLANT DOSE VS. THRESHOLD VOLTAGE AND HOLDING VOLTAGE (AS THE L_{Pad} BE EQUAL TO 10.8 UM)

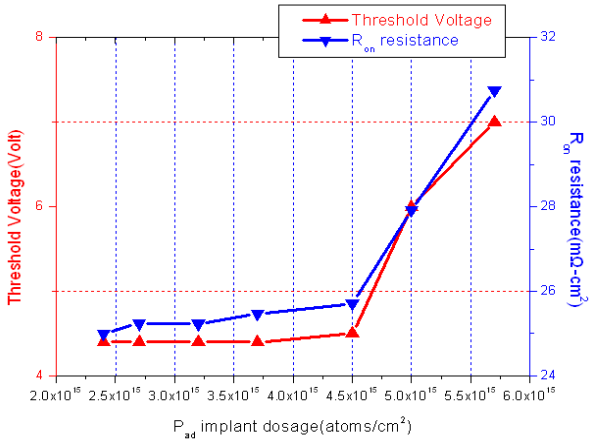

FIG. 6. CHARACTERISTICS OF P_{ad} IMPLANT DOSE VS. THRESHOLD VOLTAGE AND R_{ON} RESISTANCE (AS THE L_{Pad} BE EQUAL TO 10.8 UM)

2) Effect of the L_{Pad} Length

In Figs 7 and 8, by increasing an L_{Pad} length, i.e. the lengths of the P^+/N^+ regions are kept the same, changing L_{Pad} varies the P^- buffer layer extension length under the channel, which can raise holding

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voltage. However, the threshold voltage and R_{on} resistance were varied with the P_{ad} mask length too. The P^+/N^+ contacts were all wrapped in the P_{ad} layer in which the length will be equal to 12 μm. Additionally, the threshold voltage will be increased significantly as the L_{Pad} is equal to 10.9 μm, which is due to the status of channel region influenced by a higher P_{ad} dosage. The longer P_{ad} affects the channel region status significantly. It can be concluded that the P_{ad} structure at the N^+/P_{base} junction can prevent the LU effect, meanwhile, the R_{on} resistance and threshold voltage will be higher with a longer P_{ad} mask in the source end. So that the best condition in this situation, the L_{Pad} length is equal to 10.8 μm.

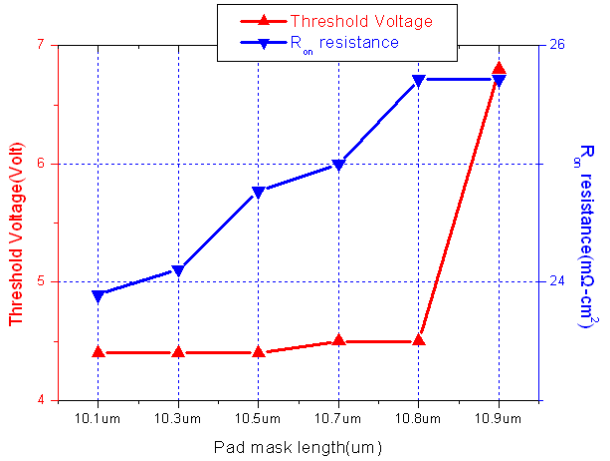

FIG. 7. CHARACTERISTICS OF P_{ad} MASK LENGTH VS. THRESHOLD VOLTAGE AND R_{ON} RESISTANCE (AS THE DOSE OF P_{ad} IMPLANT BE EQUAL TO 4.5×10^{15} ATOMS/CM²)

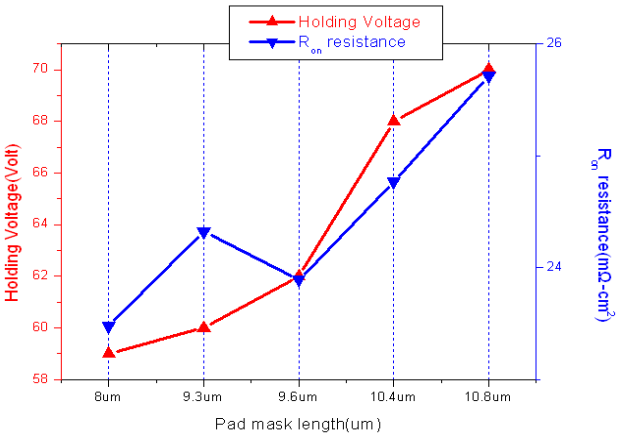

FIG. 8. CHARACTERISTICS OF P_{ad} MASK LENGTH VS. HOLDING VOLTAGE AND R_{on} RESISTANCE (AS THE P_{ad} DOSE OF IMPLANT BE EQUAL TO 4.5×10^{15} ATOMS/CM²)

Drain-side Engineering of an nLDMOS

1) Effect of the Nad Implant Dose

Furthermore, an N_{ad} implant dose and a length L_{ad} of adaptive layer in the drain side are added. The holding voltage (V_h) of an nLDMOS is raised by an N_{ad} implant dose. A RESURF (Reduce Surface Field) method is used to reduce the drain-side electric field. The junction concentration gradient of N^+/N_{epi} in the drain side is extremely high as for a conventional nLDMOS, so that the N^+/N_{epi} junction becomes breakdown easily under an ESD event. Therefore, a new N_{ad} layer was created to reduce the drain side high electric field. Such that this $N^+/N_{ad}/N_{epi}$ structure will be with two parasitic junctions. It may be regarded as two parasitic diodes that increase high-voltage endurance by this structure used to avoid the Kirk effect as an N_{ad} layer was created too. If the N^+/N_{epi} junction breakdown occurs, a high current will be produced to turn on a parasitic bipolar-junction-transistor (BJT), and which may lead to a latch-up failure. It is obvious that the holding voltage of an nLDMOS can be increased by increasing an N_{ad} implant dose as shown in Fig. 9. As the dose of N_{ad} implant was much lower, such as the N_{ad} dosage below 1.7×10^{15} atoms/cm², a double snapback characteristic is found in this structure. Due to the vertical junction-depth X_j that was shallow, a high electric field will approach N^+/N_{ad} and N_{ad}/N_{epi} junctions, eventually. Then, a higher N_{ad} dosage will be with no double snapback behavior. But, the trigger voltage is also increased with the rising of N_{ad} implant dose as well. Finally, the best condition of this N_{ad} was equal to 5.5×10^{15} atoms/cm² while the L_{ad} was fixed at 5 μm. Meanwhile, the holding voltage and trigger voltage are 97 V and 156 V, respectively. Therefore, it was a novel effective method to increase holding voltage and avoid latch-up effect in an HV nLDMOS. And, the ESD protection window is seem to be shifted to right hand in this experiment. These data can demonstrate that the holding voltage was increased by increemnt of N_{ad} implant dose significantly as shown in Fig. 9.

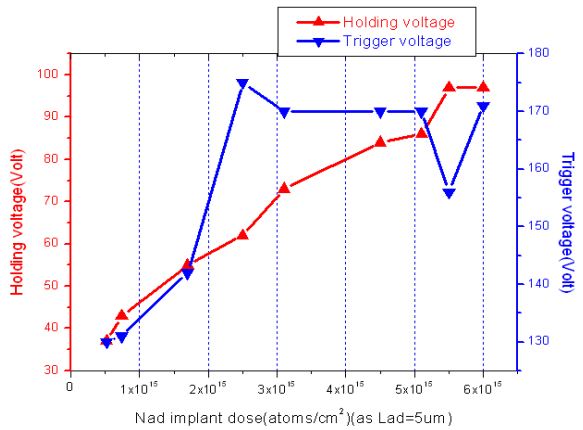

FIG. 9. EFFECT OF THE N_{ad} IMPLANT DOSE (AS L_{ad}=5 UM)

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2) *Effect of the L_{Nad} Length*

According to experiment results of the previous N_{ad} implant dose, a trigger voltage was also increased by an N_{ad} implant dose. At the same time, it can lead to internal circuit's damage before this nLDMOS device turned on under an ESD event. From Fig. 10, the trigger voltage can be reduced by increasing the mask length of L_{Nad}, i.e. the length of the N^+ region is kept the same, changing L_{Nad} varies the N^- buffer layer extension length under the LOCOS. When an L_{Nad} was fixed at 5 μm, the high electric field was found near to the N^+ region of drain side.

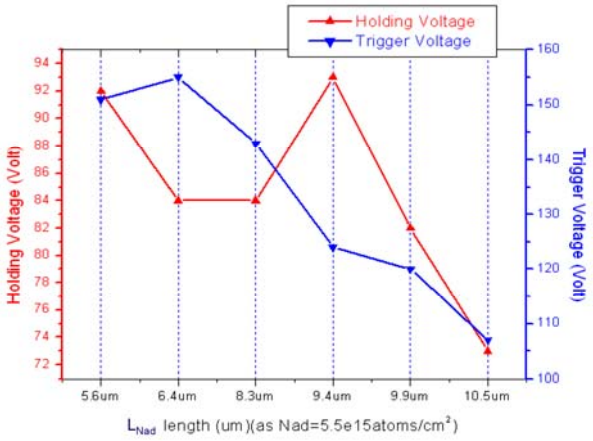

FIG. 10. EFFECT OF THE MASK LENGTH L_{Nad} (AS N_{ad}= 5.5×10^{15} ATOMS/CM^2)

When the L_{Nad} was increased from 5 μm to 10.5 μm, a high electric field was reduced in the drain side. The trigger voltage can be reduced by increasing the L_{Nad} parameter. Then, the R_{on} resistance is decreased as well, see Fig. 11. The best condition of L_{Nad} is equal to 9.4 μm while the N_{ad} implant dose is set to be 5.5×10^{15} atoms/cm^2 in the experiment, and the trigger voltage and holding voltage are 124 V and 93 V, respectively.

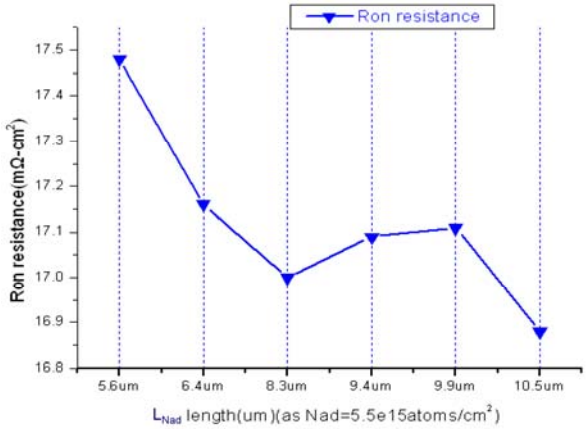

FIG. 11. R_{ON} RESISTANCE VS. MASK LENGTH OF L_{Nad} (AS N_{ad}= 5.5×10^{15} ATOMS/CM^2)

Results and Discussion

Source-side Engineering of an nLDMOS

From Figs 12 and 13, the current flow lines of an nLDMOS in different P_{ad} implant dosages, the channel surface with a crowding current density when it is with a lightened P_{ad} implant dosage, but an nLDMOS structure will be not turned on as a P_{ad} implant with a heavily dosage such as 5×10^{15} cm^{-2}. However, the P_{ad} layer will be reduced to be a surface electric-field distribution especially for some peak values at the source region as shown in Figs 14~16. A higher electric-field peak appears while the gradient of dope concentration is larger, meaning that N^+/P_{ad} and P_{ad}/P_{base} junction diodes have a higher capability against a punch-through phenomenon and sharing the potential drops. Such that a P_{ad} layer in the source ends has some advantages in the high voltage operation.

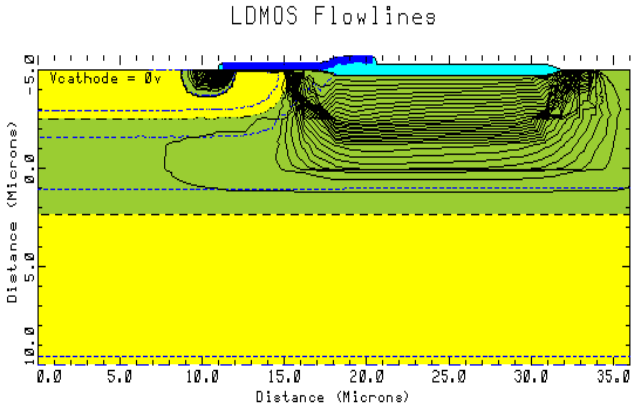

FIG. 12. ON-STATE CURRENT FLOW LINES OF AN NLDMOS UNDER V_g= 5 V, V_{DS}= 30 V (AS P_{ad} IMPLANT= 4.5×10^{15} ATOMS/CM^2, L_{Pad}= 10.8 UM)

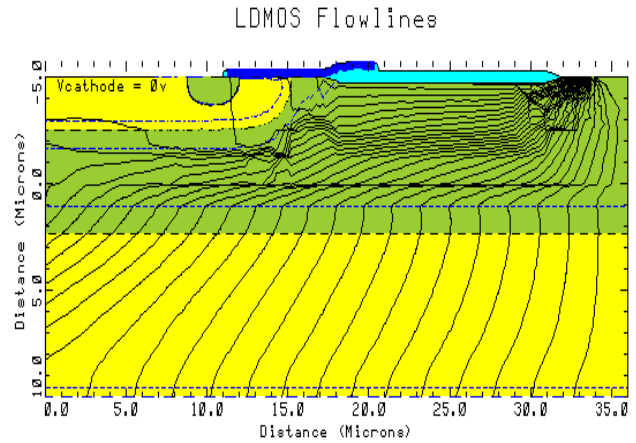

FIG. 13. ON-STATE CURRENT FLOW LINES OF AN NLDMOS UNDER V_g= 5 V, V_{DS}= 30 V (AS P_{ad} IMPLANT= 5×10^{15} ATOMS/CM^2, L_{Pad}= 10.8 UM)

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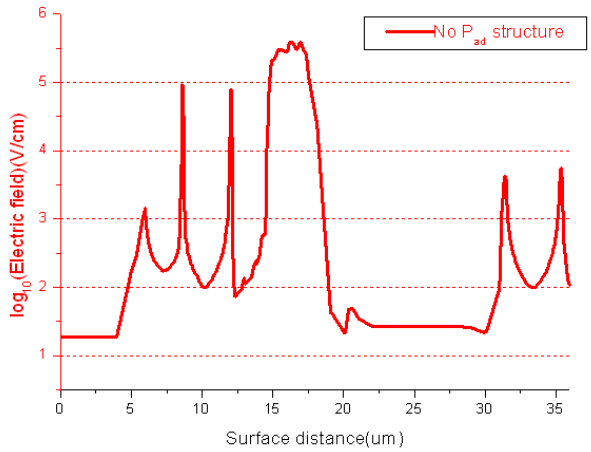

FIG. 14. SURFACE ELECTRIC FIELD DISTRIBUTION OF A CONVENTIONAL NLDMOS STRUCTURE

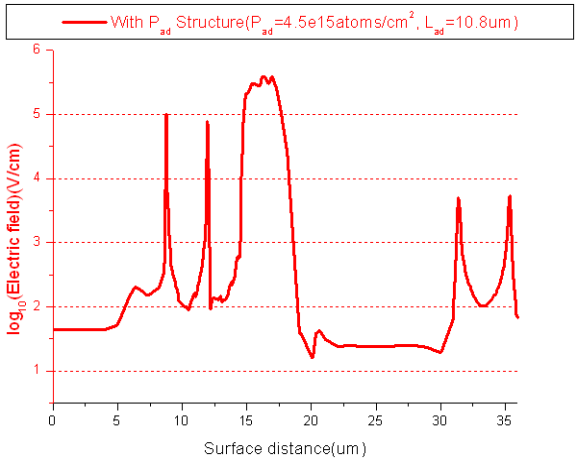

FIG. 15. SURFACE ELECTRIC FIELD DISTRIBUTION OF AN NLDMOS WITH LIGHTENED DOPING P_{ad} STRUCTURE

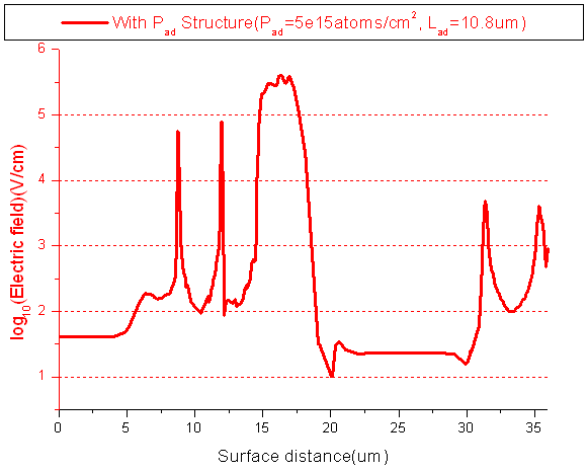

FIG. 16. SURFACE ELECTRIC FIELD DISTRIBUTION OF AN NLDMOS WITH HEAVILY DOPING P_{ad} STRUCTURE

Right-shifting characteristics of snapback I-V curves in different P_{ad} implant dosages as a length of L_{Pad} fixed at 10.8 μm are shown in Fig. 17. Obviously, the holding voltage is increased with the P_{ad} implant. Previously the double snapback characteristic was observed due to the drain side; however, the double snapback behaviour was obvious on these four curves in Fig. 17. Moreover, the double snapback I-V curves are right shifted with a P_{ad} implant too. In addition, latch-up key parameters are listed in Table. 1, and a conventional nLDMOS has a smaller holding voltage. Therefore, from Table 1, the best condition of V_{t1} and V_h are 125 V and 70 V, respectively.

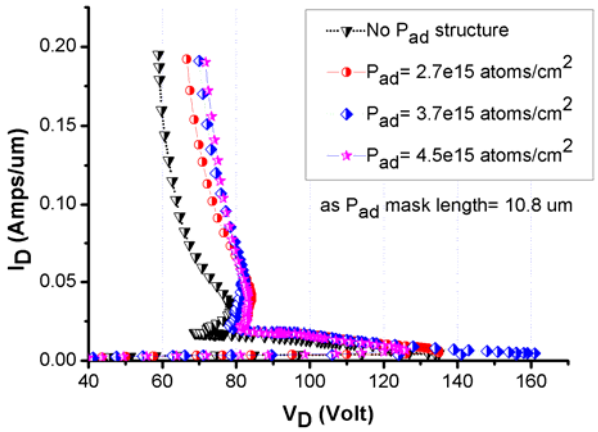

FIG. 17. RIGHT-SHIFTING CHARACTERISTICS OF SNAPBACK I-V CURVES IN DIFFERENT P_{ad} IMPLANT DOSAGES

TABLE 1. THE COMPARISON OF SNAPBACK PARAMETERS DURING DIFFERENT P_{AD} IMPLANT DOSAGES

	V_{t1} (Volt)	V_h (Volt)
Conventional	135	58
P_{ad} implant= 2.7×10^{15} atoms/cm^2, L_{Pad}= 10.8 μm	135	65
P_{ad} implant= 3.7×10^{15} atoms/cm^2, L_{Pad}= 10.8 μm	160	67
P_{ad} implant= 4.5×10^{15} atoms/cm^2, L_{Pad}= 10.8 μm	125	70

Drain-side Engineering of an nLDMOS

Figs 18~20 show the surface electric-field distribution of an nLDMOS as the bias condition was stressed under V_g= 5 V and V_{DS}= 40 V. In Fig. 18, the electric field of none with N_{ad} structure in the drain side has reached about 10^4 V/cm, therefore, the N^+/N_{epi} junction was easy breakdown under this high electric field. Fortunately, from Fig. 19, an N_{ad} structure can share the high electric field of drain side and decrease more significantly one order magnitude. If we enlarge the length of L_{Nad}, the high electric field near the drain-side will be reduced as shown in Fig. 20. Therefore, by this technique, the surface field at the drain side is successfully lowered. It can be concluded that the N_{ad} structure can avoid a parasitic junction-diode

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breakdown of $N^+/N_{ad}/N_{epi}$ and suppress the Kirk effect efficaciously.

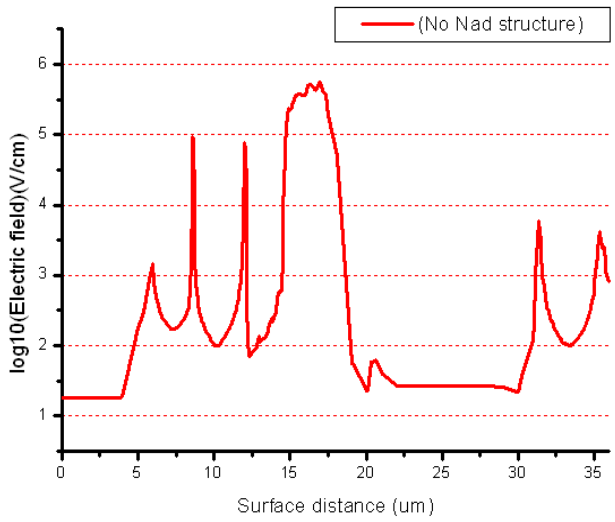

FIG. 18. SURFACE ELECTRIC FIELD DISTRIBUTION WITH A NONE N_{ad} STRUCTURE

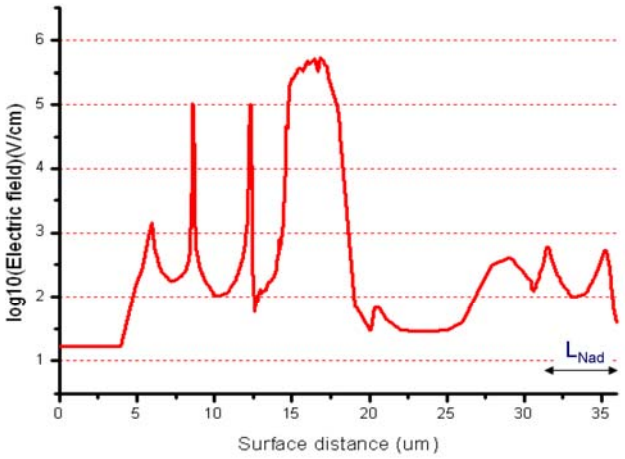

FIG. 19. SURFACE ELECTRIC FIELD DISTRIBUTION WITH AN N_{ad} STRUCTURE (AS N_{ad}= 5.5×10^{15} ATOMS/CM^2, L_{Nad}= 5 UM)

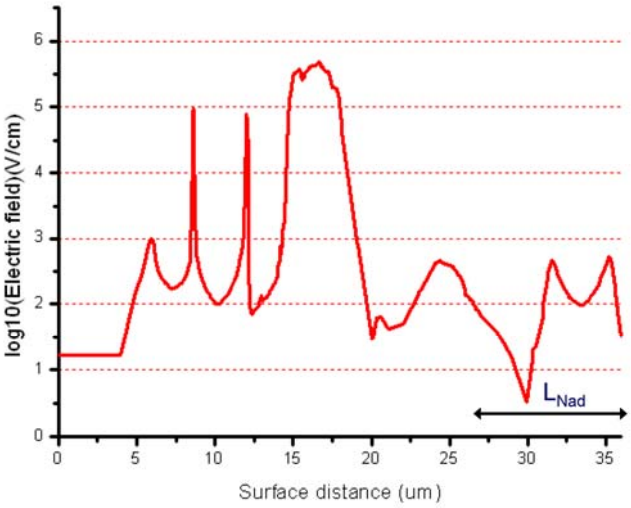

FIG. 20. SURFACE ELECTRIC FIELD DISTRIBUTION WITH AN N_{ad} STRUCTURE (AS N_{ad}= 5.5×10^{15} ATOMS/CM^2, L_{Nad}= 9.4 UM)

From Fig. 21, the snapback I-V curve is right shifted while increasing the N_{ad} implant dosage. As the concentration gradient of N_{ad}/N_{epi} junction becomes large, then it leads to a high electric field moved from N^+/N_{ad} to N_{ad}/N_{epi}. Two junction diodes can sustain a higher voltage stress, such that the holding voltage of an nLDMOS is increased by raising the N_{ad} implant dosage. It can be observed that the trigger voltage is also increased by raising the N_{ad} implant dosage as well. Therefore, the latch-up reliability issue of an nLDMOS can be easily overcome with an N_{ad} doping technique in the drain side.

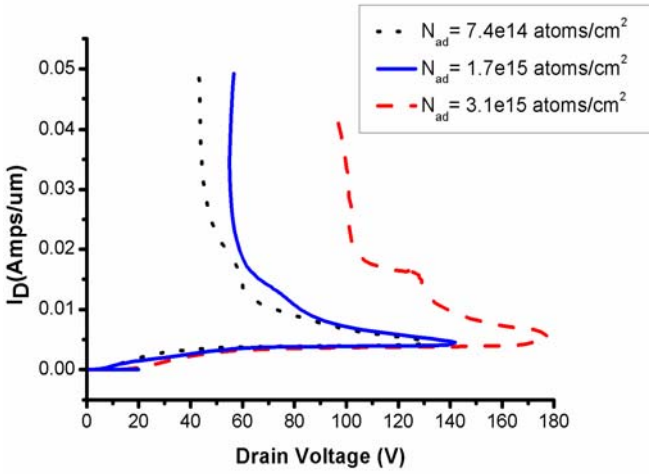

FIG. 21. RIGHT-SHIFTING CHARACTERISTICS OF SNAPBACK I-V CURVES IN DIFFERENT N_{ad} IMPLANT DOSAGES (AS THE L_{Nad}= 5 UM)

Furthermore, snapback I-V curves of three different structures are shown in Fig. 22, in which the black dot line is a conventional structure of nLDMOS. It's apparent that it has the lowest holding voltage and holding current as compared with the other two. The blue dash line is an effective method to increase the holding voltage and the snapback I-V curve is right shifted significantly. Finally, the red solid line is an optimization result in this work, and it is with a much higher V_h and the lowest V_{t1} values. This work succeeds to realize a weak snapback characteristic of nLDMOS. Such that this methodology has an excellent LU capability to avoid latch-up disaster and with a much higher robustness to protect internal circuits under an ESD event. Consequently, from Table 2, the best condition of V_{t1} and V_h are 124V and 93V, respectively. Accordingly, both good for the reliability design window by this drain-side engineering are due to a decrement 7 V (5.3%) of the V_{t1} and an increment 21 V (29.2%) of the V_h.

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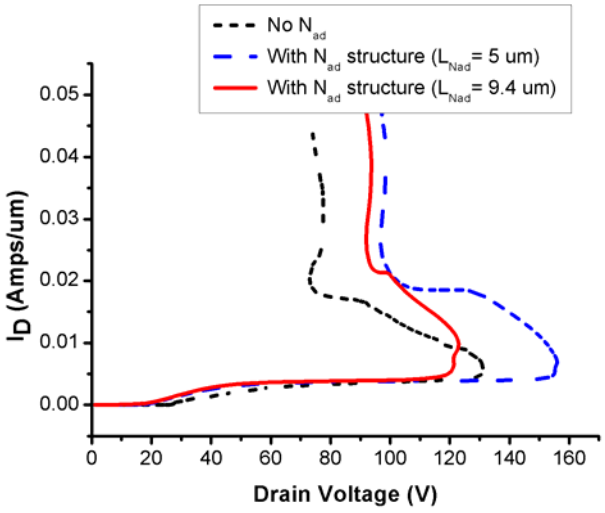

FIG. 22. RIGHT-SHIFTING CHARACTERISTICS OF SNAPBACK I-V CURVES IN DIFFERENT L_{Nad} WIDTHS (AS THE N_{ad}= 5.5×10^{15} ATOMS/CM^2)

TABLE 2. THE COMPARISON OF SNAPBACK PARAMETERS DURING DIFFERENT L_{NAD} WIDTHS

	V_{t1} (Volt)	V_h (Volt)
No N_{ad}	131	73
N_{ad}= 5.5x10^{15} atoms/cm^2 L_{Nad}= 5 μm	156	97
N_{ad}= 5.5x10^{15} atoms/cm^2 L_{Nad}= 9.4 μm	124	93

Conclusion

In this work, a weak snapback of an nLDMOS has been presented. The source/drain engineering can suppress substrate noise and prevent latch-up effect. The peak value of surface electric field can be reduced by these two junction diodes N^+/P_{ad} and P_{ad}/P_{base} or N^+/N_{ad} and N_{ad}/N_{epi} successfully. And, the latch-up issue can be easily solved by these methodologies in a high voltage operation. So, it's a novel method to reduce the surface field, control the trigger voltage and holding voltage. Obviously, the holding voltage is increased and an improvement of LU reliability can be achieved. The right-shifting characteristic of snapback I-V curves depends on P_{ad}, L_{Pad}, N_{ad}, and L_{Nad}, respectively. Eventually, it is found that a more robustness characteristic of LU reliability can be obtained by inserting these new adding P_{ad}/N_{ad} layers in the source/drain sides. It can be concluded that a novel source/drain engineering to achieve weak snapback nLDMOS by the adaptive layer for HV power applications in which both the suitable trigger voltage and holding voltage can be realized easily. From the above analysis, if it is both with N_{ad}/P_{ad} structures, the nLDMOS can increase holding voltage more effective to ensure reliability capability in many kinds of applications. Thus, it is very easy to fine tuning the trigger voltage and the holding voltage by using these adaptive layers variations.

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